What is claimed is:

1. A memory device, comprising:

a data line; and

a variable delay precharge circuit that receives a column bank address signal and a write enable signal and that precharges the data line responsive to the column bank address signal at a time that is determined by a state of the write enable signal.

2. The memory device of Claim 1, wherein the variable delay precharge circuit comprises:

a precharge circuit operative to precharge the data line responsive to a precharge control signal;

a variable delay precharge control signal generator circuit that receives the column bank address signal and the write enable signal and that delays the precharge control signal with respect to the column bank address signal responsive to the write enable signal.

3. The memory device of Claim 2, wherein the variable delay precharge control signal generator circuit comprises:

a precharge control signal generator circuit that receives the column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column address bank signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to the write enable signal.

4. The memory device of Claim 1, wherein the variable delay precharge circuit precharges the data line after a first predetermined time period following assertion of the column bank address signal when the write enable signal indicates a read operation, and wherein the variable delay precharge circuit precharges the data line after a second predetermined time period following assertion of the column bank address signal when the write enable signal indicates a write operation.

5. The memory device of Claim 4, wherein the second time period is shorter than the first time period.

6. A memory device comprising:

a pair of data input/output lines;

a precharge circuit that precharges the pair of data input/output lines responsive to a precharge control signal;

a precharge control signal generator circuit that receives a column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time periods with respect to the column address bank signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to a write enable signal.

7. The memory device of claim 6, wherein the first precharge control signal rises in synchronization with a rising edge of the column bank address signal and falls the first period of time after an immediately succeeding falling edge of the column bank address signal, and wherein the second precharge control signal rises in synchronization with a rising edge of the column bank address signal and falls the second period of time after an immediately succeeding falling edge of the column bank address signal.

8. The memory device of claim 6, wherein the pair of data input/output lines are a pair of global input/output lines of the memory device.

9. A precharge control circuit for controlling a precharge circuit of a semiconductor memory device, the precharge control circuit comprising:

a precharge control signal generator circuit that receives a column bank address signal, that generates first and second delayed signals from the column address bank signal that are delayed by respective different first and second time

periods, and that applies, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to a write enable signal,

wherein the precharge delay control circuit causes application of the first precharge control signal after a read operation of the memory device and application the second precharge control signal after a write operation of the memory device.

10. The precharge control circuit of claim 9, wherein the first period of time is longer than the second period of time.

11. The precharge control circuit of claim 9, wherein the control circuit comprises:

a first delay that receives the write enable signal and outputs an inverted delayed signal therefrom;

a NOR circuit that receives the write enable signal and the inverted delayed signal output from the first delay, performs a NOR operation on the write enable signal and the inverted signal, and responsively outputs a signal; and

a latching/inverting circuit that receives, latches, and inverts the signal output from the NOR circuit and the first delay signal, and responsively outputs a signal.

12. The precharge control circuit of claim 11, wherein the first delay comprises an odd number of inverters connected in series.

13. The precharge control circuit of claim 9, wherein the precharge control signal generator circuit comprises:

a first NOR circuit that receives the second delay signal and the signal output from the latching/inverting circuit, performs a NOR operation on the second delay signal and the signal output from the latching/inverting circuit, and responsively outputs a first signal;

a second NOR circuit that receives the column bank address signal and the first delay signal, performs a NOR operation for the column bank address signal and the first delay signal, and responsively outputs a second signal; and

a third NOR circuit that receives the first and second signals output from the first and second NOR circuits, performs a NOR operation on the first and second signals, and responsively outputs a third signal.

14. The precharge control circuit of claim 13, wherein, if the write enable signal indicates a write operation, the precharge control signal generator circuit generates the first precharge control signal, and wherein, if the write enable signal indicates a read operation, the precharge control signal generator circuit generates the second precharge signal.

15. A method of generating a precharge control signal for a precharge circuit of a memory device, the method comprising:

receiving a column bank address signal;

generating first and second delayed signals from the column bank address signal that are delayed respective first and second time periods;

logically OR'ing the column bank address signal and the first delayed signal to generate a first signal;

logically OR'ing the column bank address signal and the second delayed signal to generate a second signal;

generating one of a first precharge control signal responsive to the first signal and a first state of a write enable signal; and

generating a second precharge control signal responsive to the second signal and a second state of the write enable signal,

wherein the first time period is greater than the second time period.

16. The method of claim 15, wherein the first precharge control signal is generated responsive to a read operation of the memory device, and wherein the second precharge control signal is generated responsive to a write operation of the memory device.